REMARKS

Claims 1-16 are pending in the present application. Claims 1, 2, 6, 9, 10, 12 and 14 have been amended.

Priority Under 35 U.S.C. 119

The Examiner is respectfully requested to acknowledge receipt of the English language translation of foreign language U.S. Provisional Application Serial No. 60/413,753, as filed along with the present application, and to confirm that the Claim for Priority under 35 U.S.C. 119(e) is complete.

Claim Objections

Claim 12 has been objected to in view of the informality as listed on page 2 of the current Office Action dated September 14, 2004. Claim 12 has been corrected as suggested by the Examiner. The Examiner is therefore respectfully requested to withdraw this objection.

Claim Rejections-35 U.S.C. 112

Claims 6 and 14 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claims 6 and 14 have been amended to delete "type", to be in better compliance with 35 U.S.C. 112, second paragraph. The Examiner is therefore respectfully requested to withdraw this rejection.

Claim Rejections-35 U.S.C. 102

Claims 1-6 and 9-14 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Orii et al. reference (U.S. Patent No. 5,559,464). This rejection is respectfully traversed for the following reasons.

The voltage level shifting circuit of claim 1 includes in combination a complimentary signal input circuit "which is coupled to the first power supply node and which includes a pair of first MOS transistors, each of the first MOS transistors has a first withstand voltage and has a first electrode coupled to the first power supply node, a second electrode, and a gate electrode receiving one of the complimentary signals"; a load circuit "which is coupled to the third power supply node and which includes a pair of second MOS transistors, each of the second MOS transistors has a second withstand voltage higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode"; and a third MOS transistor "which is coupled between the third power supply node and an output node, which has the second withstand voltage, and which electrically connects the third power supply node to the output node in response to a voltage potential output from the load circuit...". Applicant respectfully submits that the Orii et al. reference as relied upon by the Examiner does not disclose these features.

As described in column 12, lines 57-61 of the Orii et al. reference, when transistor Q1 is on, transistor Q1 remains in the 3v voltage tolerance range. As described in column 13, lines 3-7 of the Orii et al. reference, transistor Q11 also

remains in the 3v voltage tolerance range. As described in column 13, lines 30-31 of the Orii et al. reference, transistor Q31 remains in the 3v voltage tolerance range. Transistors Q2, Q3 and Q4 are variously described in column 13, line 52 through to column 14, line 17 of the Orii et al. reference, as remaining in the 3v voltage tolerance range. As further described in column 14, lines 21-23 of the Orii et al. reference, all of the MOS transistors that comprise mediator signal generator circuit 2 are within the 3v voltage tolerance range. As described in column 15, lines 34-49 and 56-61, MOS transistors Q8, Q81, Q71 and Q7 of output buffer circuit 3 are in the 3v voltage tolerance range.

Since all of the transistors in Fig. 1 of the Orii et al. reference are described as being within a same 3v voltage tolerance range, the Orii et al. reference as relied upon by the Examiner does not disclose a load circuit including a pair of second MOS transistors that have a second withstand voltage higher than a first withstand voltage, as would be necessary to meet the features of claim 1. The Orii et al. reference as relied upon by the Examiner also fails to disclose a third MOS transistor coupled between a third power supply node and an output node, which has a second withstand voltage. Applicant therefore respectfully submits that the voltage level shifting circuit of claim 1 distinguishes over the Orii et al. reference as relied upon by the Examiner, and that this rejection of claims 1-6 is improper for at least these reasons.

Applicant also respectfully submits that the voltage level shifting circuit of claim 9 distinguishes over the Orii et al. reference as relied upon by the Examiner for at least

somewhat similar reasons as set forth above. The Orii et al. reference as relied upon by the Examiner does not disclose a load circuit including a pair of second MOS transistors each having a second withstand voltage higher than a first withstand voltage, and a third MOS transistor coupled between a third power supply and an output node that has a second withstand voltage, as would be necessary to meet the features of claim 9. Applicant therefore respectfully submits that the voltage level shifting circuit of claim 9 distinguishes over the Orii et al. reference as relied upon by the Examiner, and that this rejection of claims 9-14 is improper for at least these reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 7, 8, 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. However, Applicant respectfully submits that claims 7, 8, 15 and 16 should be allowable at least by virtue of dependency upon claims 1 and 9 respectively, and that further amendment of these claims to be in independent form is thus unnecessary.

Conclusion

Applicant respectfully submits that the claims have been amended merely to improve form, rather than to further distinguish over the relied upon prior art. That is, the claims distinguish over the prior art as relied upon by the Examiner for the reasons

as set forth above. Accordingly, the corresponding amendments to the claims should not be construed as narrowing scope within the meaning of *Festo*.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

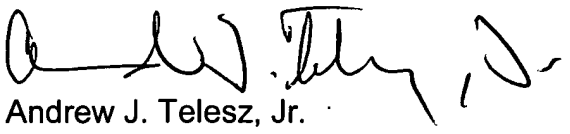
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of two (2) months to February 14, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of $450.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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